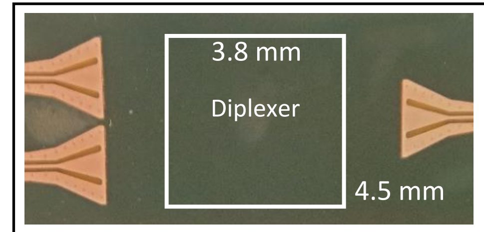
BT LAMINATE E-BAND DIPLEXER, 71 – 86 GHZ

General Description:



EDIP7186-R05 is the first commercial E-band diplexer manufactured in a low CTE BT resin laminate for IC plastic packages (FCCSP, BGA, CSP, SiP, etc.), ideally suited for *low-cost* and *high-volume* production – enabling smaller and cheaper last-mile links and small-cells. The diplexer has a low passband of 71 to 76 GHz and a high passband of 81 to 86 GHz with an insertion loss of 3 dB (typ.), a return loss of at least 15 dB, and cross-over suppression of more than 20 dB. The minimum isolation in an adjacent channel is 55 dB. The diplexer boasts a form-factor of 3.8 x 4.5 mm, thus making it the smallest planar E-band diplexer on the market. Bare-die ICs may be placed above the diplexer, allowing for tight integration of an entire E-band front-end as a SoC. Custom IC land-patterns and BGA mappings may be requested – in addition to the available sample design.

The common port has a WR-12 transition for integration with waveguide antennas, while the two channels are provided as CPW transitions, for IC flip-chip / wire-bond integration.

Features:

- Manufactured in a low CTE BT resin laminate for IC plastic packages (FCCSP, BGA, CSP, SiP, etc.)
- Low cost, high volume
- Small form-factor (3.8 x 4.5 mm)
- High out-of-band suppression (55 dB +)
- High return loss (15 dB +)
- Attractive insertion loss (3 dB typ.)

Applications:

- Last-mile point-to-point E-band links
- E-band front-haul
- E-band small-cells & μ-cells

Electrical Specifications:

Parameter	Minimum	Typical	Maximum
Low passband (LB)[1] frequency	71 GHz		76 GHz
High passband (HB)[2] frequency	81 GHz		86 GHz
Passband insertion loss		3 dB	
Passband return loss	15 dB		
Rejection / channel isolation	55 dB		
Cross-over suppression		20 dB	
Group delay variation		125 ps	
Power handling		1 W (CW)	
Specification temperature		+25 °C	
Operating temperature	-40 °C		+85 °C

[1,2] LB and HB relative channel locations are shown in Figure 3.

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Mechanical Specifications:

Item	Specification
Common port	WR-12 waveguide port opening.
Channel ports	CPW for flip-chip or wire-bonding with target die. AC coupled.
Material	Low CTE BT resin laminate + copper. RoHS compliant.
Finish	OSP Gen 3 + soldermask if necessary, as per customer requirements.
Weight	< 5 g
Diplexer size	3.8 (L) x 4.5 (W) x 0.8 (H) mm, see Figure 3 for details.
Package size	9.45 (L) x 8.0 (W) x 1.2 (H) mm, see Figure 3 for details.

Measured response (60 – 110 GHz)[3]:

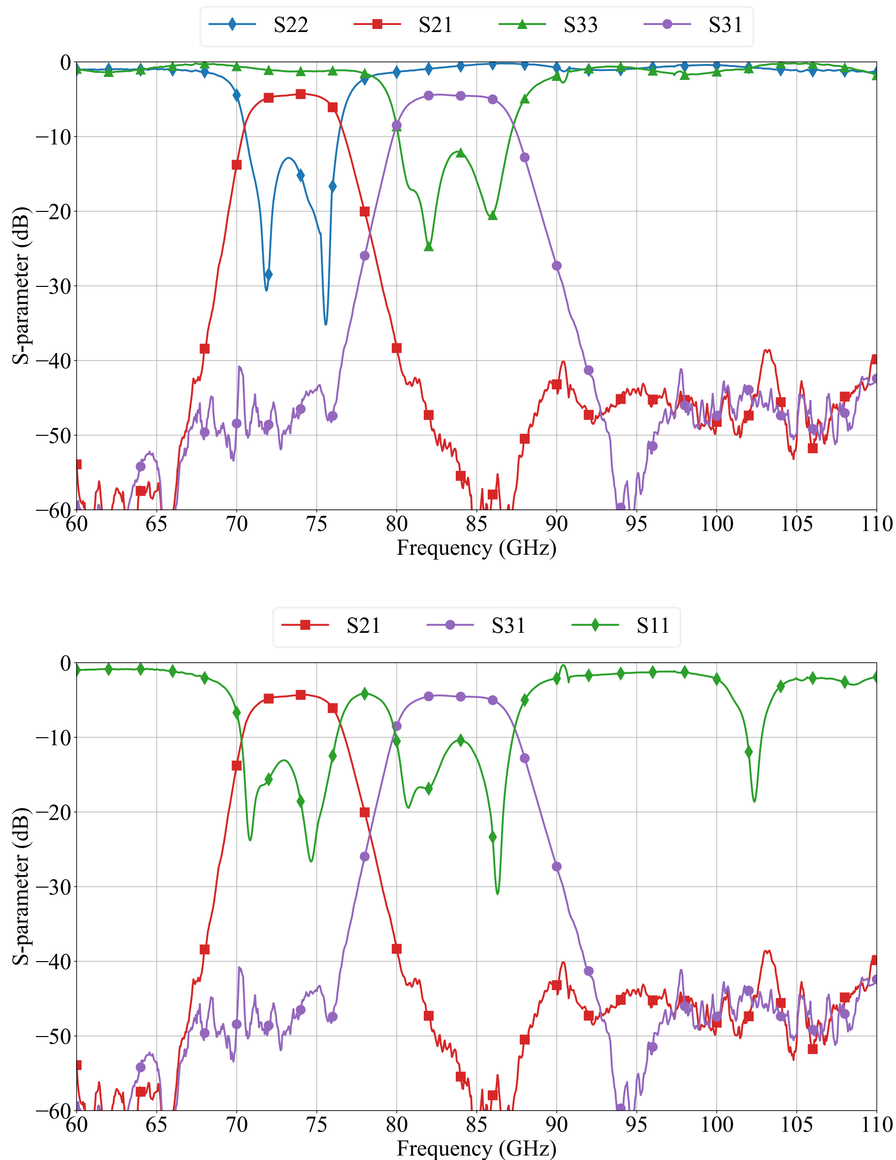

Figure 1. Measured S-parameter response over the range: 60 – 110 GHz.

[3] Please note that presented measurements are preliminary and may differ from the Electrical Specifications. Measurements are expected to match specifications with future iterations. Isolation will be 55 dB (min).

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EDIP7186-R05, BT LAMINATE E-BAND DIPLEXER

Measured response (10 – 110 GHz):

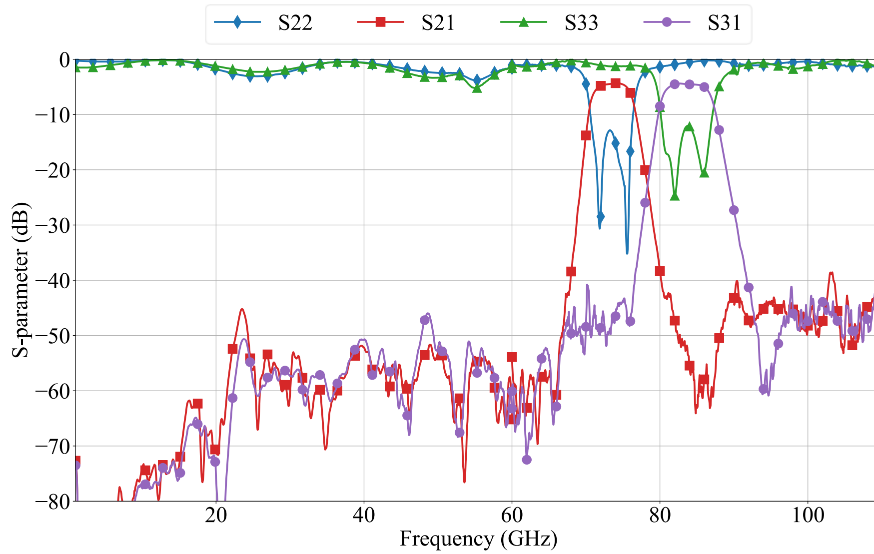

Figure 2. Measured transmission S-parameter response over the range: 10 – 110 GHz.

Outline dimensions[4] & recommended footprints:

The package outline, not including bare-die ICs is shown below. Bottom pads and diplexer / WR-12 transition locations are also shown.

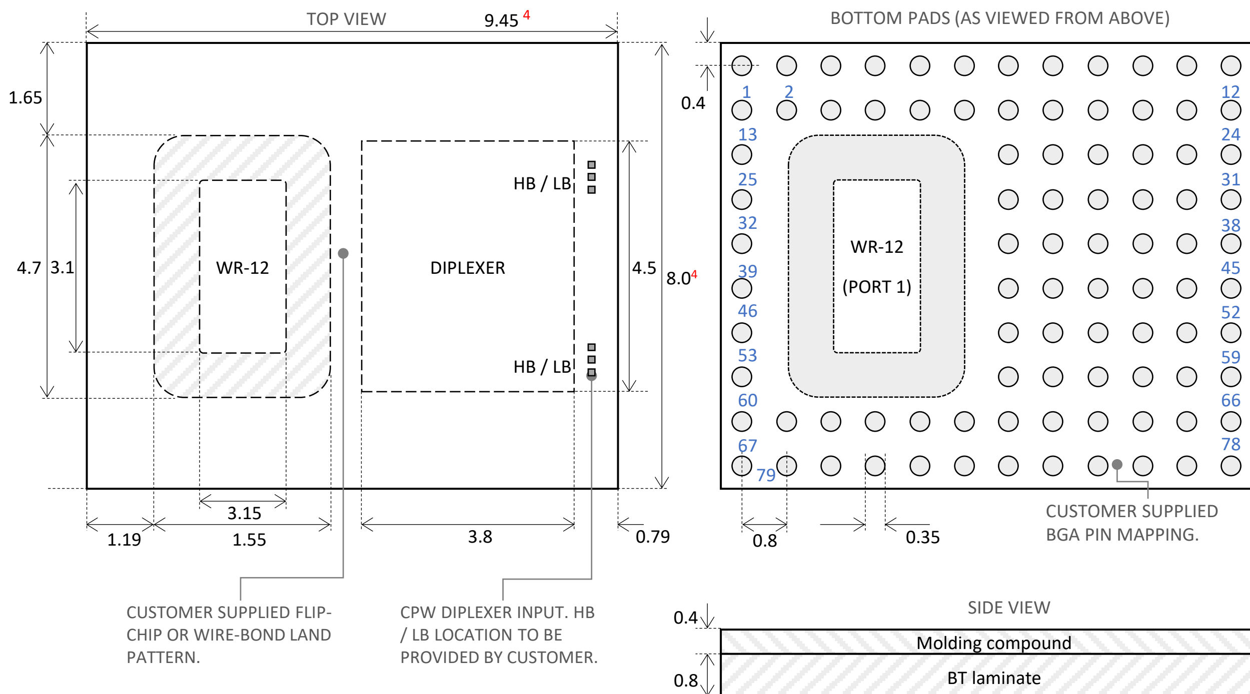

Figure 3. Package outline and bottom land-pattern.
Dimensions in millimetres.

[4] Package dimensions can be adjusted based on customer requirements and choice of bare-die ICs.

Typical application layout

An example application SoC front-end integrated with the BT laminate diplexer is shown in Figure 4. Analog Devices[5] bare-die ICs are used. Design data and samples are available upon request.

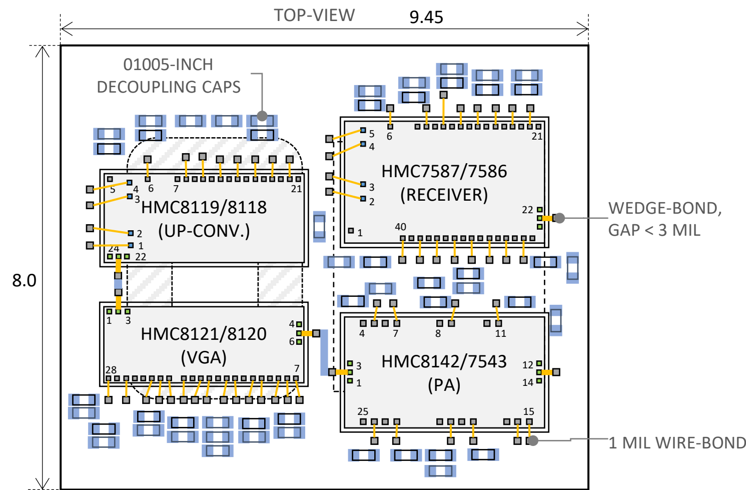

Figure 4. Example application land pattern using Analog Devices bare-die ICs.
Dimensions in millimetres.

Typical pin configuration:

The pin mapping is configurable by the customer as it depends on the chosen bare-die ICs. The customer is to provide the required IC land-pattern, the desired BGA pin configuration as well as the electrical connections between the two. Routing will then be proposed in discussion with the customer. The table below shows the BGA pin configuration for the typical application layout above (also refer to Figure 3).

Pin no.	Mnemonic	Description
2, 4, 7, 12-14, 18, 19, 22, 23, 28-31, 35-38, 40-42, 44, 49, 51, 53-56, 58, 64-66, 69, 74-78, 85, 90	GND	Ground connections. These pins must be connected to RF & DC ground.
	EXP_PADS	Exposed pads are connected to ground.
	RX-chain	
26, 27, 33, 34	RX _IP, RX_IN, RX_QP , RX_QN	Positive/negative IF RX in-phase (I) and quadrature (Q) inputs.
24	RX_LO	LO input (RX chain).
21	RX_MIX_VG	Gate voltage for the Field Effect Transistor (FET) mixer (RX chain).
8, 20, 9	RX_AMP_VD12, RX_AMP_VG	Drain/gate voltages for the LO amplifier (RX chain).
45, 47, 48, 52, 59	LNA_VG12, LNA_VD34, LNA_VG34, LNA_VD12	Gate/drain voltages for the various stages of the LNA (RX chain).

[5] Analog Devices components are the property of Analog Devices, Inc.

10, 11	RX_MUL_VD, RX_MUL_VG	Gate/drain voltages for the LO multiplier (RX chain).
	TX-chain	
25, 32, 39, 46	TX_IP, TX_IN, TX_QP, TX_QN	Positive/negative IF TX in-phase (I) and quadrature (Q) inputs.
6	TX_LO	LO input (TX chain).
1	TX_MIX_VG	Gate voltage for the FET mixer (TX chain).
3, 15, 16	TX_AMP_VD12, TX_AMP_VG	Drain/gate voltages for the LO amplifier (TX chain).
5, 17	TX_MUL_VG, TX_MUL_VD	Drain/gate voltages for the LO multiplier (TX chain).
60, 67, 79, 68, 70, 82, 71, 72, 81, 83	VGA_VG12, VGA_VD12, VGA_CTL12, VGA_VD345, VGA_VD6, VGA_VG34, VGA_VG56	Gate/drain voltages for the VGA (TX chain).
43, 50, 57, 61, 62, 63, 86, 87	PA_VD34, PA_VD12, PA_VG12, PA_VG34	Gate/drain voltages for the PA (TX chain).
73, 80, 84	VGA_VDET, VGA_ENV, VGA_VREF	Reference and output voltages for the VGA power detector (TX chain) and envelope detector.
88, 89	PA_VREF, PA_VDET	Reference and output voltages for the PA power detector (TX chain).

Note:

- All data presented was collected from a sample lot. Actual data may vary from unit to unit.
- Multifractal Semiconductors (Pty) Ltd reserves the right to change the information presented without notice.
- Flip-chip land pattern as well as BGA pin function are to be provided by the customer – based on this data routing from the ICs to the BGA pins will be proposed.

Caution:

- This product is under development and therefore technical parameters and measurements are expected to improve. Presented data is preliminary data.

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